WHAT IS CLAIMED IS:

1. A method for determining a bit error rate in an input data stream received on an integrated circuit, comprising:

determining over a plurality of first time intervals whether at least one transition of the input data stream occurred in a predetermined phase zone of a sample clock used to sample the input data stream; and

generating a count value according to how many of the first time intervals have at least one transition that occurred in the predetermined phase zone, the count value corresponding to the bit error rate.

2. The method as recited in claim 1 wherein the count value is generated over a second time interval that includes the plurality of first time intervals.

3. The method as recited in claim 1 wherein determining the bit error rate comprises:

generating a second count value over a third time interval that includes a plurality of second time intervals, thereby providing better accuracy for low bit error rates.

4. The method as recited in claim 1, further comprising supplying a bit error rate indication corresponding to the count value via at least one output terminal of the integrated circuit.

5. The method as recited in claim 4 wherein the bit error rate indication supplied has a value that corresponds to a range of count values.

6. The method as recited in claim 4 wherein the bit error rate indication is an analog signal supplied from the one output terminal of the integrated circuit, a level of the analog signal indicative of the bit error rate.

7. The method as recited in claim 6 wherein the analog signal is a current.

8. The method as recited in claim 1 further comprising:

assigning a digital value that corresponds to the count value;
supplying the digital value to a digital to analog converter;
converting the digital value to an analog signal; and
supplying on an output terminal of the integrated circuit the analog signal, thereby indicating the bit error rate according to a level of the analog signal.

9. The method as recited in claim 1 further comprising:
asserting an output signal on an output terminal of the integrated circuit if the bit error rate is above a threshold value.

10. The method as recited in claim 9 further comprising:
receiving an analog signal on an input terminal of the integrated circuit, a level of the analog signal indicative of the threshold value.

11. A method for determining if a phase-locked loop in an integrated circuit receiving an input data stream remains locked to a timing of the input data stream, the method comprising:
determining over a plurality of first time intervals whether at least one transition of the input data stream occurred in a predetermined phase zone of a sample clock used to sample the input data stream;
generating a count according to how many of the first time intervals have at least one transition that occurred in the predetermined phase zone; and
evaluating whether the phase-locked loop remains locked to the timing of the input data stream according to the count.

12. The method as recited in claim 11 further comprising providing a signal indicating a loss of lock condition if the count exceeds a predetermined threshold.

13. An integrated circuit:
means for detecting transitions of the input data stream occurring in a predefined phase zone of a sample clock sampling the input data stream; and

means for determining a bit error rate according to how many of a plurality of evaluation intervals have one or more transitions in the predefined phase zone.

14. The integrated circuit as recited in claim 13 further comprising:

means for supplying on an output terminal of the integrated circuit an indication of the bit error rate, the indication corresponding to the number of evaluation intervals that have one or more transitions that fall into the predefined phase zone.

15. A method of determining a bit error rate of an input data stream, comprising:

determining whether transitions of the input data stream fall into a predetermined portion of a sample clock period of a sample clock utilized to sample the input data stream; and

determining a bit error rate according to how many of a plurality of evaluation intervals have one or more transitions in the predetermined portion of the sample clock period.

16. The method as recited in claim 15, wherein the sample clock is a clock recovered from the input data stream.

17. The method as recited in claim 15, wherein the determining includes generating a count indicative of how many of the evaluation intervals have at least one transition in the predetermined portion of the clock period, and supplying a bit error rate indication corresponding to the count.

18. The method as recited in claim 17, further comprising converting the count to a digital value corresponding to one or more count values.

19. The method as recited in claim 17 wherein the predetermined portion of the clock period is adjacent to a clock edge used to sample the input data stream.

20. A method of making a tested integrated circuit comprising:

supplying an input data stream to the integrated circuit;

determining whether transitions of the input data stream fall into a predetermined portion of a sample clock period of a sample clock utilized to sample the input data stream;

determining how many of a plurality of evaluation intervals have one or more transitions in the predetermined portion of the sample clock period and supplying an indication thereof; and

monitoring the indication to determine satisfactory performance of the integrated circuit.

21. The method as recited in claim 20 wherein the input data stream is supplied with varying data rates to test a frequency range of the integrated circuit.

22. The method as recited in claim 20 wherein the input data stream is supplied with varying amounts of jitter to test jitter tolerance of the integrated circuit.

23. An integrated circuit for receiving an input data stream, the integrated circuit comprising:

a bit error detect circuit coupled to determine if a bit error occurs in the input data stream according to whether an input data stream transition occurs in a predetermined phase zone of a sample clock used in the bit error detect circuit; and

a counter circuit coupled to the bit error detect circuit to supply an indication of a number of evaluation intervals in which at least one bit error occurs.

24. The integrated circuit as recited in claim 23 wherein:

the bit error detect circuit includes a first data path and a second data path coupled to receive the input data stream, one of the first and second data paths being delayed with respect to the other, thereby defining the phase zone, and wherein respective output signals from the first and second data paths are coupled to a logic circuit to be logically compared.

25. The integrated circuit as recited in claim 23 wherein the first data path is part of a phase detector circuit coupled to provide an indication of phase error between a recovered clock being used to sample the input data stream and the input data stream.

26. The integrated circuit as recited in claim 24 wherein the one of the first and second data paths is delayed by delaying one of the clock and the data of the input data stream supplied to the one path.

27. The integrated circuit as recited in claim 23 wherein the second data path includes one or more selector circuits to select from a plurality of clock frequencies.

28. The integrated circuit as recited in claim 24 wherein the respective output signals from the first and second data paths are logically compared in an exclusive OR circuit.

29. The integrated circuit as recited in claim 23 further comprising:
an output terminal supplying a digital signal indicative of a bit error rate, the output terminal being part of a communication port, the bit error rate being determined according to how many of the evaluation intervals have at least one bit error.

30. The integrated circuit as recited in claim 23 further comprising:
an output terminal supplying an analog signal indicative of a bit error rate, the bit error rate being determined according to how many of the evaluation intervals have at least one bit error.

31. An integrated circuit for determining an out-of-lock condition with respect to an input data stream, the integrated circuit comprising:
a phase zone detect circuit coupled to determine if a transition of the input data stream occurs in a predetermined phase zone of a sample clock used to sample the input data stream;

a counter circuit coupled to the phase zone detect circuit to supply a count indication of how many of a predetermined number of evaluation intervals have at least one transition that occurs in the predetermined phase zone; and

a compare circuit coupled to compare the count indication to a predetermined value to determine if a phase-locked loop remains locked to a timing of the input data stream.

32. The integrated circuit as recited in claim 31 wherein each of the evaluation intervals comprises multiple bit times of the input data stream.